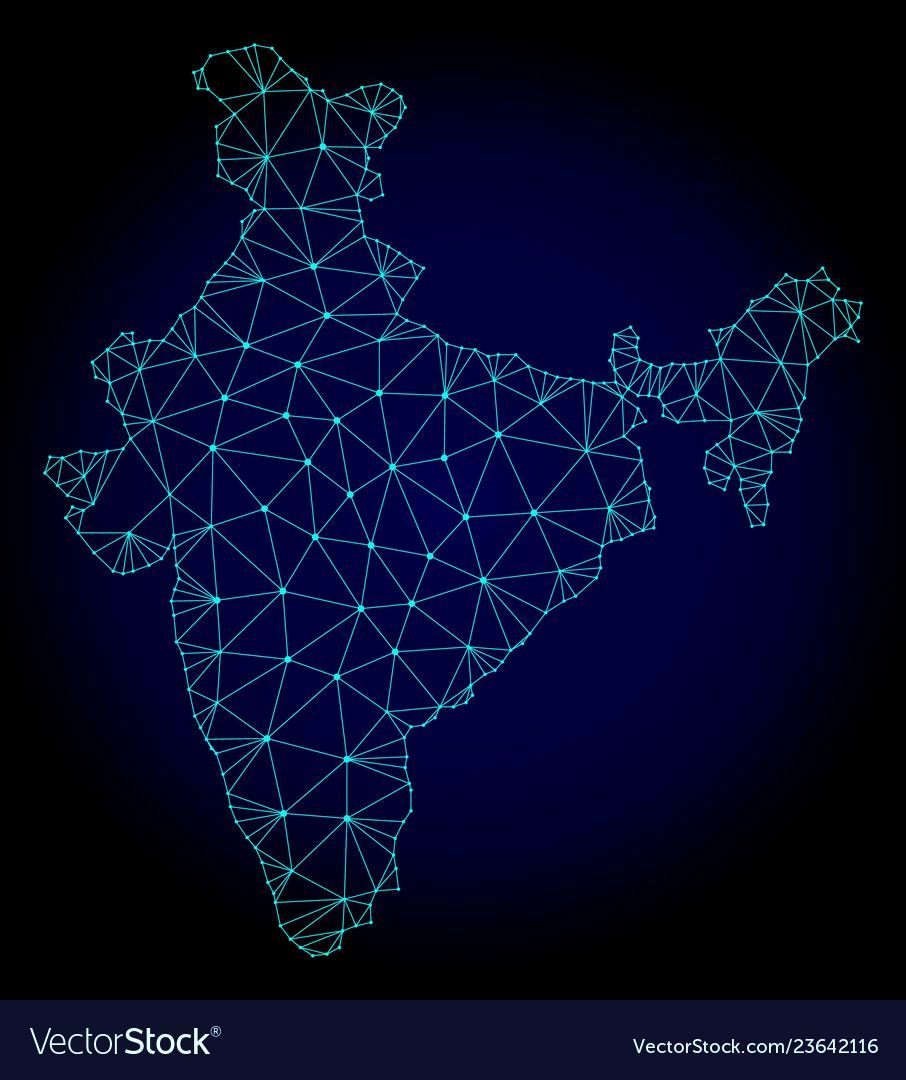
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**Next Gen Courses in Design, Semiconductors, Packaging and Systems to Educate Students and Industry Professionals**

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**Fundamentals of System Design & Architectures**

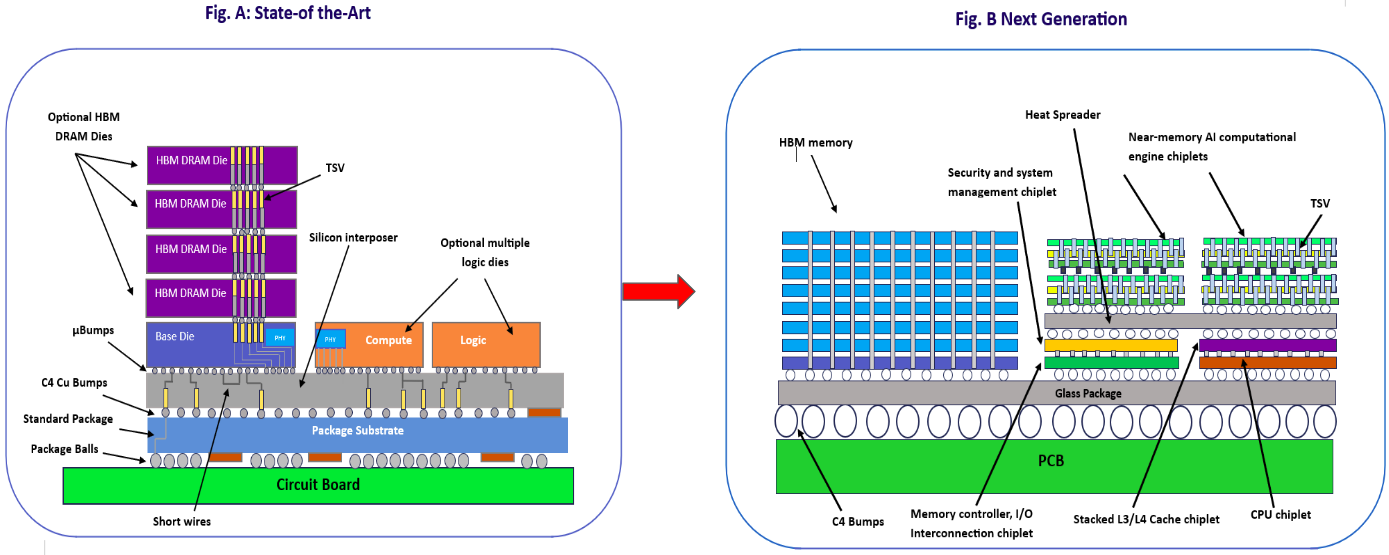
**Course Instructor: Prof. Binod Kumar, IIT Jodhpur**

**Course Content:** With the increased demand of high-performance computing with high bandwidth, next-generation system architectures (such as heterogeneously integrated packages) have become necessary to meet the higher throughput at lower energy. Workloads (eg. AI models) keep growing in complexity requiring new architectures, posing a multitude of challenges that can only be solved through a variety of innovative solutions such as multiple IP integration, hardware-software co-design methodologies and scalable interconnect designs. This course describes techniques for designing high-performance AI accelerator architectures and hardware- software co-design methodologies that can lead to implementation of reconfigurable and energy-efficient core designs. To meet these challenges, chiplet-based designs are becoming increasingly popular for next -gen high performance systems. The course also describes design space exploration methodology for 3D-chiplet-based system settings to obtain suitable parameter values for optimization of factors such as power dissipation, latency, number of communication links and overall area consumption. The course, in addition, also discusses methods of minimizing the system latency while maximizing the overall system throughput, two essential characteristics of chiplet-based system designs for a range of applications including computationally-intensive AI workloads.

**Course for Graduate Students and Industry Professionals:** This course is designed for both

undergraduate and graduate students as well as working professionals. The course will initiate

participants to the rudiments of system design methodology and then take a deep dive into some of the advanced topics.



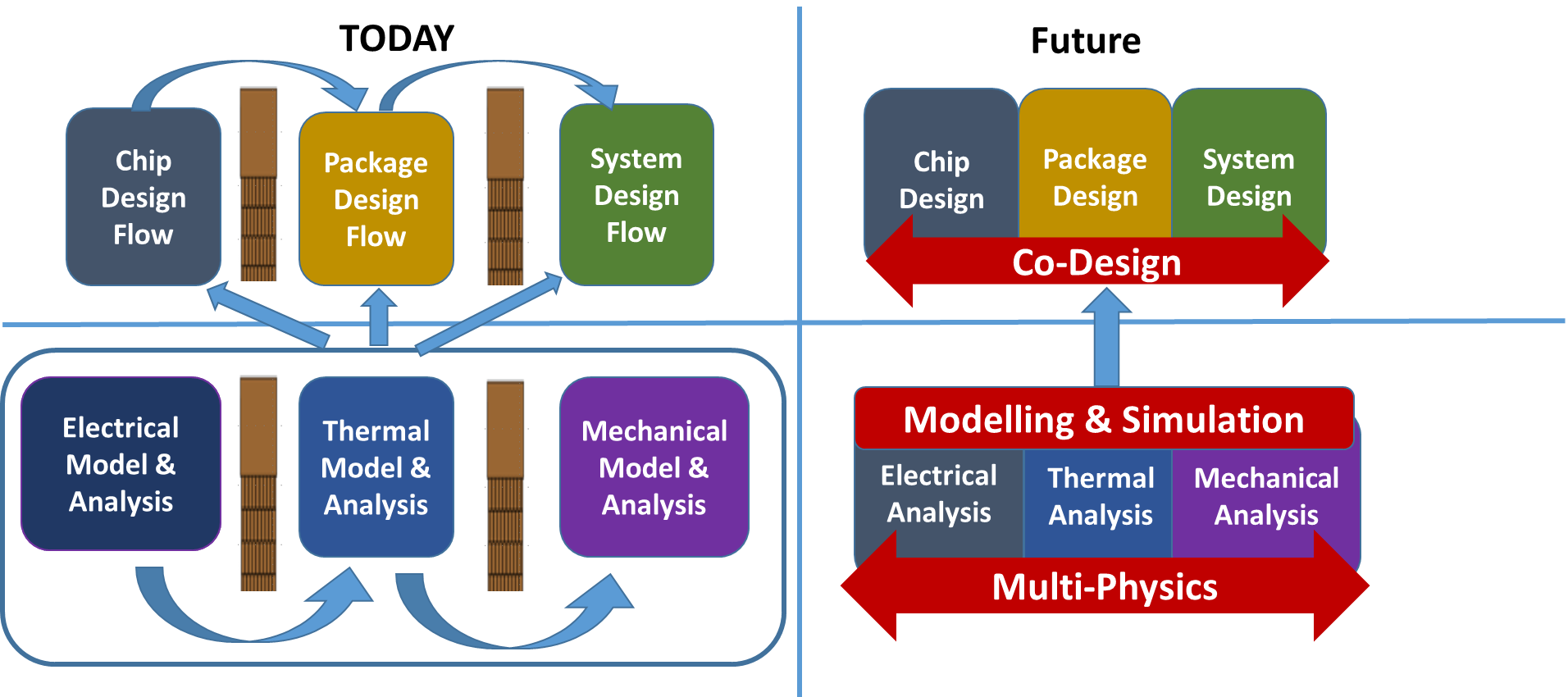
**Fig.1 System Architectures for HPC and AI : Past and Future**

**Fundamentals of Chip-Package Co-Design**

**Course Instructor: Prof. Rohit Sharma, IIT Ropar**

**Course Content**: Advanced computing and high-speed wireless communications have necessitated highly integrated packages to meet the higher throughput at lower energy. This is very different from the past of advancing each component and integrating all components on system boards. The new design focus therefore is on integrated chip-package co-design for performance and power efficiency.  
  
The course starts with the fundamentals of chip design starting with classical MOS technologies and then covers advanced device and circuit technologies for the AI era. Key performance metrics including power, delay, area, and cost will be analyzed from one technology node to another. Participants will get a clearer understanding of the design tradeoffs as a function of integrated package architectures, BEOL technologies, and surface and grain boundary scatterings, the latter significantly degrading the electrical performance and aggravating thermal and reliability. Carbon and 2D materials such as nanoscale graphene are potential solutions as next gen on-chip interconnects owing to their outstanding electrical and thermal properties.  
  
At the package level, this course focuses on four major design areas, namely signal integrity, power delivery, EMI/EMC and co-design of all these at combined chip and package levels. The course focuses on fundamentals of signal and power integrity, and the role of codesign for achieving better electrical-thermal-mechanical performance and reliability. The course also covers fundamentals of chip-to-chip signaling, design of high-speed interconnects; analysis of transmission lines and the associated signal integrity challenges including delay, crosstalk, noise and eye diagrams. The practical aspects of power design, delivery, distribution and the importance of signal and power supply noise will be covered.

**Course for Grad Students and Industry Professionals**: This course is designed for both undergrad and graduate students as well as working professionals. The course will initiate participants to the rudiments of package design and then take a deep dive into some of the advanced topics.

 **Co-Design for next generation heterogeneously integrated packages and systems**

**Fundamentals of CMOS Devices**

**Course Instructor: Prof. Nihar Ranjan Mohapatra, IIT Gandhinagar**

**Course Content**: The evolution of CMOS technology has been the driving force behind the digital revolution, enabling exponential growth in computing power and energy efficiency. However, as the industry approaches the physical and economic limits of Moore's Law, the need for innovative approaches to overcome scaling- performance bottlenecks has never been more critical. This short course, is designed to provide a comprehensive overview of how CMOS technology has evolved, and the cutting-edge advances and emerging paradigms that are shaping the future of the semiconductor industry.

The course will begin by tracing the journey of CMOS evolution, from traditional planar MOSFETs to the introduction of FinFETs and Nanosheet FETs, which have redefined performance benchmarks. It will then explore the exciting potential of Complementary FETs (CFETs) and stacked CMOS technologies, which promise unprecedented transistor integration density and energy efficiency. Particular focus will be placed on Gate-All-Around (GAA) architectures, which are becoming critical for sub-3nm nodes, along with the advent of multi-patterning lithography techniques, including EUV lithography, and their role in pushing scaling limits. Participants will also be introduced to the role of power-performance-area-cost (PPAC) optimization, and how design-technology co-optimization (DTCO) is reshaping the industry.

**Course for Grad Students and Industry Professionals**: This course is designed for students, researchers, and professionals eager to stay at the forefront of semiconductor technology. By the end of this course, participants will have a good understanding of the state-of-the-art in CMOS advancements, the strategic shifts required to address future challenges, and the exciting opportunities that lie ahead for the semiconductor industry. This knowledge will empower participants to learn and contribute meaningfully to the design, development, and application of future-generation semiconductor technologies, to contribute in an ever-evolving technological landscape.

A diagram of a graph

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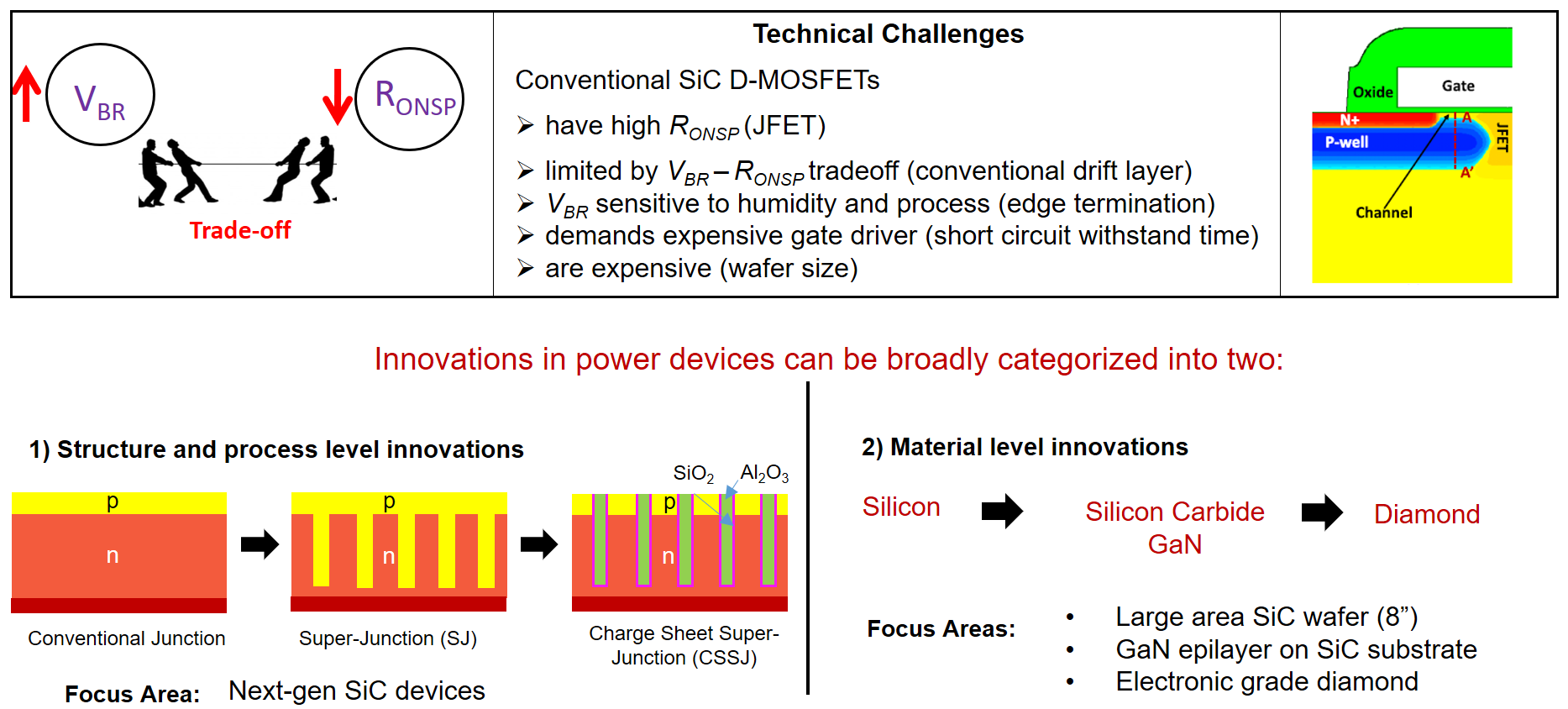
**Fundamentals of Power Devices**

**Course Instructor : Prof. Akshay K (IIT Bhubaneswar)**

**Course Content**: With the advent of advanced power electronic applications such as electric automobiles, renewable energy management, motor drives in industrial and consumer electronics, smart grid systems etc., the demand for low-loss power semiconductor devices with high voltage and faster switching is dramatically increasing. This course shall discuss the uniqueness of discrete power devices over other semiconductor devices used in memory or processors. Further, some of the important static, dynamic, thermal and reliability parameters of a power MOSFET will be reviewed and important considerations involved in its design will be discussed. Key recent research innovations aimed at breaking the *Silicon limit* (trade-off between breakdown voltage and specific on-resistance) will also be discussed such as use of wide bandgap semiconductors and use of novel device structures like super-junctions.

**Course for Grad Students and Industry Professionals**: This course is designed for students, researchers, and professionals who are eager to get introduced to the area of discrete power devices. By the end of this course, participants will be able to Understand the uniqueness of discrete power devices and read the data sheet of a power MOSFET and identify a few critical parameters as well as understand the techniques used in breaking *Silicon limit. In addition, the participants will*understand the advantages of wideband gap semiconductors and super-junction structures in power devices.

This knowledge will lay a foundation for the participants motivating them to learn more and contribute meaningfully to the design, development, and application of future-generation power semiconductor device technologies.



**Fundamentals of Electronic Interconnecting Substrates**

**Course Instructor: Prof. Pradeep Dixit, IIT Bombay**

**Course Content: **Substrates interconnect one or more chips on a single unit. This interconnection requires multiple layers of wiring either on the surface or inside the substrate. They play a crucial role, therefore, in determining the performance, reliability, and miniaturization of modern electronic devices. These substrates serve as a platform on which various active and passive components including integrated circuits (ICs), resistors, capacitors, etc., can be interconnected electrically. In addition, substrates provide mechanical support, electrical pathways, heat dissipation, and signal and power integrity. Depending on the specific I/O needs, substrates can be either plastic, ceramic, organic, silicon or glass substrates

This course aims to educate the students and industry professionals about this rapidly evolving field of interconnecting substrates used in semiconductor packaging and thus is ideal for professionals seeking to enhance their skills in the semiconductor industry. Fundamentals and advanced concepts of substrate technologies, focusing on their critical role in supporting high-performance, miniaturization, and reliability will be covered. Details of various substrates, including, lead-frame, ceramic organic, alumina, silicon, and glass interposers, along with advanced fabrication techniques such as through substrate vias (TSV), RDL and other High-Density Interconnects (HDI). The course will also cover the critical substrate properties for thermal management, electrical performance, and mechanical stability. The current status and upcoming challenges in this domain will be covered.

**Course for Grad Students and Industry Professionals:**

This course is designed for students, researchers, and professionals interested in learning about the technical aspects of substrates used in semiconductor packaging. By the end of this course, participants will have a good understanding of various types of substrates, important material properties, key fabrication processes, and their usage in applications including in automotive, 5G, High-Performance Computing (HPC) etc.

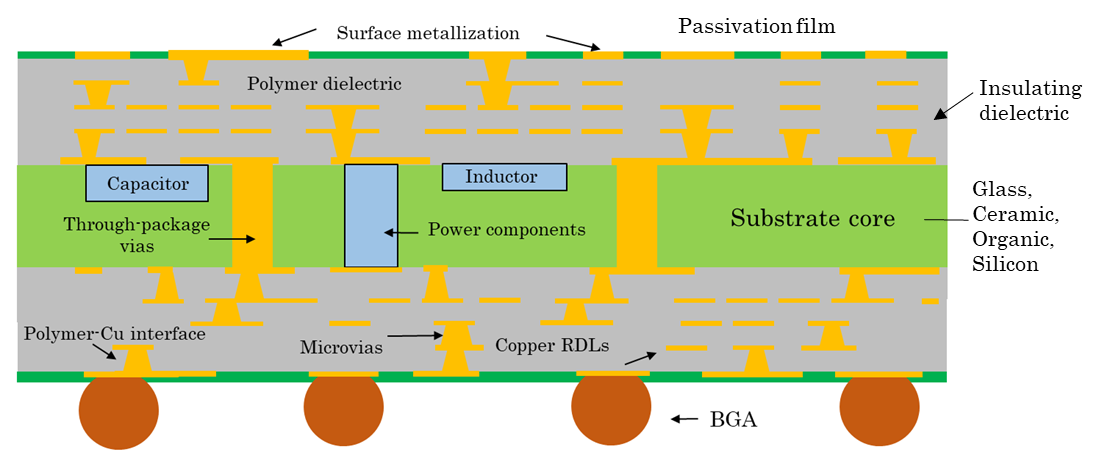


Figure: Next generation Substrate with embedded IPDs and ultrafine pitch RDLs

**Fundamentals of Co-Packaged Optics**

**Course Instructor: Prof. Naresh Emani, IIT Hyderabad**

**Course Content:**

 As the demand for higher computing performance continues to rise— driven mainly by AI workloads — conventional Moore’s Law-based devices face increasing bandwidth and power efficiency limitations. To overcome these challenges, **Co-Packaged Optics (CPO)** has emerged as a critical solution, offering significant improvements in **power consumption, bandwidth density,** and overall system performance for next-generation data centres. This course explores the key technological advancements enabling CPO, including **photonic device integration**, **high-speed photonic interconnects**, and **hybrid bonding and assembly techniques**. The CPO market is projected to grow significantly, from $95 million in 2025 to $1.2 billion by 2035, underscoring its transformative potential in high-performance computing and data centre architectures.

This course will discuss the challenges and critical technologies required to enable CPO, focusing on energy-efficient data transmission, high bandwidth packaging, and system integration approaches. Some of the critical technologies that will be discussed are:

1. System Design for ultra-high bandwidth at low power for AI applications
2. Cu-Cu hybrid bonding of ASIC-SRAM(Si-Si) and EIC-PIC (InP-Si) chiplets
3. Electrical and mechanical design and fabrication of glass interposer with photonic interconnections with fine pitch RDLs
4. Cu-Cu thermocompression bonding of HBM and ASIC chiplets on glass interposer
5. Advances in assembly to organic substrates (C2 bonds)
6. Fiber coupling with advances in automatic alignment and bonding of fibre arrays

A diagram of a structure

Description automatically generated**Course for Grad Students and Industry Professionals:** This course is designed for undergraduate and graduate students and working professionals. The course will introduce participants to the fundamentals of Co-Packaged Optics.

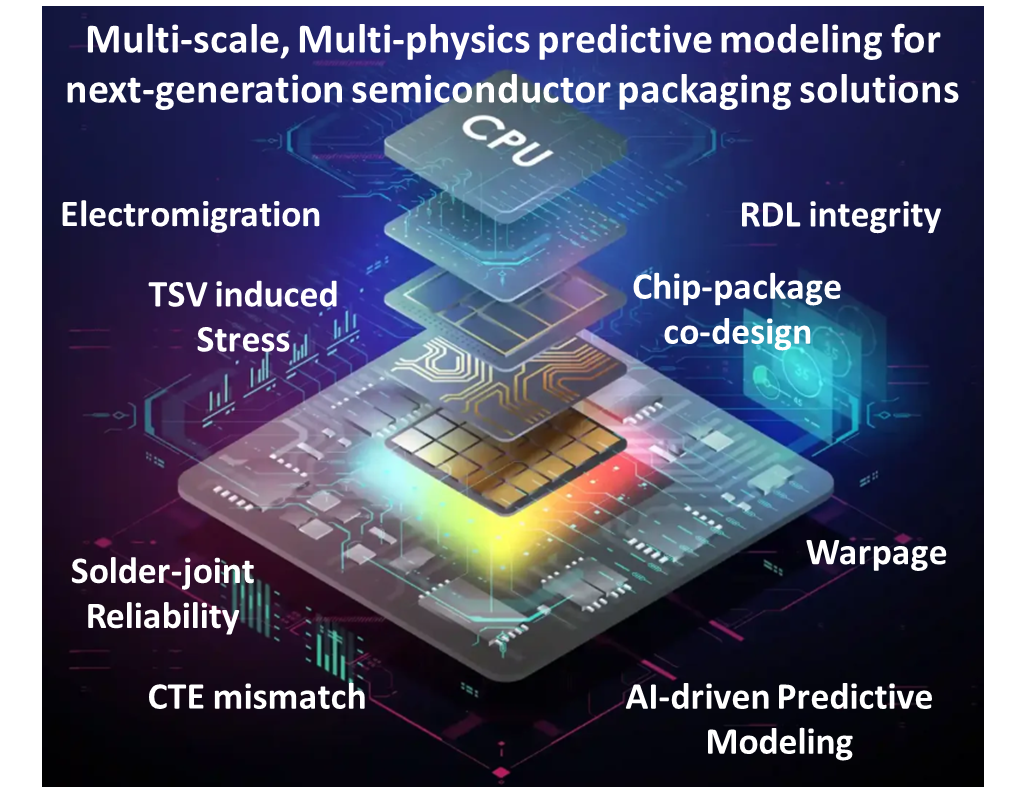
Figure: The cross-section of the proposed prototype

**Predictive Modeling and Co-Design for Advanced Semiconductor Packaging**

**Course Instructor: Prof. Tarun Kumar Agarwal, IIT Gandhinagar**

 The increasing complexity of integrated semiconductor packages, driven by package integration such as by 2.5D, 3D and chiplet architectures, has introduced significant challenges in chip-package interactions, not only electrically but mechanically as well. Traditional design methodologies often fail to account for the multi-scale, multi-physics and multi materials phenomena as systems are built with sub nano structures on the chip to 100 ‘s of micron structures on the system board..These challenges necessitate advances in predictive modeling and design approaches to design these complex packages with minimal electrical failures emanating from mechanical failure mechanisms as these new packages integrate devices, interconnecting substrates with power and embedded components and thermal structures at system-levels to design, fabricate and optimize the integrated packages for performance, reliability, power efficiency, and manufacturability.

**Course Content**: In this short course, the students learn about physics-based multi-scale modeling and co-design strategies to address key failure mechanisms in integrated packages. Topics will include thermal-mechanical reliability, focusing on warpage, through via-induced stresses, and embedded power devices and components affecting chip-package interactions. The students will also learn about electromigration and interconnect aging, particularly failures of solder joints, Cu bumps and pillar interconnects, and redistribution layers (RDLs) under high current densities expected of AI era. The discussion will extend to solder joint and underfill reliability, analyzing the impact of thermal cycling, moisture ingress, and coefficient of thermal expansion (CTE) mismatch on long-term performance. Additionally, the students will learn about future trends in predictive modeling by combining physical and data-driven modeling techniques such as reduced-Order models, Integrating digital twins, AI-driven predictive models, and physics-informed neural networks (PINNs) for accelerated design-space exploration and reliability predictions.

**Course for Grad Students and Industry Professionals**: This course is aimed at graduate students, industry professionals, and researchers working in semiconductor and package design, fabrication, and reliability. The course will provide insights into the latest methodologies and emerging research directions in multi-scale, multi-physics predictive modeling for next-generation semiconductor packaging solutions [1] K.-N. Tu, *Microelectronics Reliability*, 2011, [2] H. Kim et al.," *IEEE Transactions on CPMT*, 2023, [3] Z. Shen et al., *Applied Physics Reviews*, 2023, [4] P.-N. Hsu et al., *Scientific reports*, 2022, [5] C. Yuan et al., *IEEE EuroSim*, 2024.

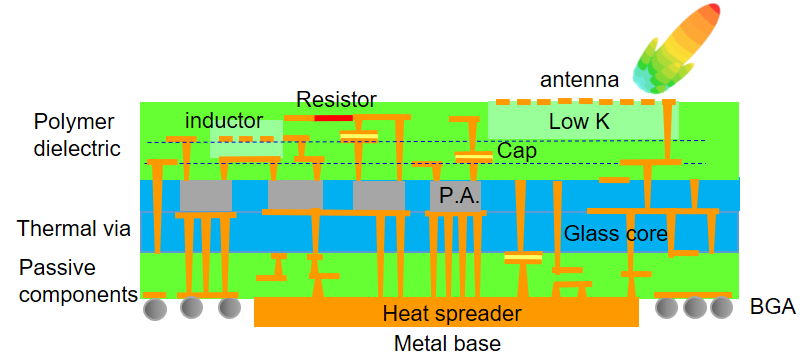
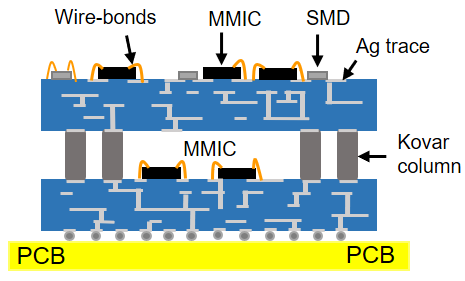
**Fundamentals of 6G Integrated Systems**

**Course Instructor: Prof. Mrinal K Mandal, IIT Kharagpur**

**Course Content**: Advancing 6G systems requires addressing technical challenges at millimeter-wave frequencies, specifically D-band frequencies (110–170 GHz) as required by the global industry, with a focus on 3D heterogeneous integration of active and passive devices. This involves a detailed analysis of signal integrity, interference, parasitic, and the development of innovative techniques for reducing signal interference, parasitic compensation, and loss reduction.

The course will begin with the fundamentals of RF and millimeter-wave engineering, focusing on challenges related to signal propagation, crosstalk, and antenna design in the D-band. 3D packaging and integration techniques for compact and efficient component placement. Advanced materials, substrates, and devices such as GaN for power amplifiers and electro-optic materials for high-speed data transmission, will be covered. A solid understanding of meta-surfaces and their design principles for controlling electromagnetic waves are critical for reducing crosstalk. Additionally, the course will cover antenna design, MIMO systems, beamforming network integration, and high-power MMIC design. Electromagnetic connection techniques, including via-pads and micro-bump technology, will be described to achieve reliable interconnects in 3D integration. The course will conclude with electromagnetic compatibility and signal integrity testing techniques for validating the performance of these complex systems.

**Course for Grad Students and Industry Professionals**: This course is designed for grad-students, researchers, and professionals eager to stay at the forefront of semiconductor technology. By the end of the course, participants will have a detailed understanding of the metrics for effective electromagnetic integration, the challenges and solutions for 3D interconnects and heterogeneous packaging, the technologies currently used to address these challenges, and the underlying physics behind them.



Present Emerging

Design and modelling

Co-design and S.I. analysis

Test, characterize, and demonstrate

**Fundamentals of MEMS & Sensor Systems**

**Course Instructors : Prof. Venkatesh Rao, BITS Pilani & Prof. Bhaskar Mitra, IIT Delhi**

 **Course Content**: MEMS is an innovative technology based on semiconductor manufacturing that has led to an entirely new kind of products in such diverse areas as inertial motion sensors, automotive sensors, Digital Micromirror Devices (DMD), microphones, ultrasound transducers, RF filters and microphones to name a few. From inkjet printheads to airbag accelerometers, MEMS have generated hockey stick growth for many companies in an era where MOORE’s law is saturating. Being a relatively low-cost technology, it is an ideal area for small, innovative companies to grow rapidly with disruptive technology. Additionally, where drones and robots are ubiquitous, MEMS are playing a critical element in performance of these systems.

The course will begin by tracing the history of MEMS – with its roots in IC technology and evolution of bulk and urface micromachining processes. After a brief discussion of MEMS processes, we will discuss the building blocks of MEMS: Beams and Flexures. Finally, the course will explore application domains using a series of case studies: Acclerometers, Gyroscopes, MEMS Switches, Resonators and Filters. We will also cover some aspects of CMOS and MEMS integration, MEMS testing, reliability and business practices.

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**Course for Grad Students and Industry Professionals**: This course is designed for students, researchers, and professionals eager to get a foothold into the area of MEMS technology. By the end of this course, participants will have a good understanding of MEMS technology Landscape, the current state of the art, and latest developments in the field. This course will empower organizations who are keen on entering into MEMS design and production to get an overview of the field and provide a base for design engineers to contribute meaningfully to their organizations.

**Materials for Devices, Components and Packaging**

**Instructors: Prof. Bhagwati P, IISc, Prof. Praveen K, IISc & Prof. Murali KP, NIT Calicut**

This short professional development course provides an overview of materials used in devices, packages, components and systems. These materials provide a variety of functions such as dielectrics, conductors, capacitors, encapsulants, photoresists and many others. The type of materials used include metals and alloys, ceramics, glasses, polymers and composites.

**Course Content: Materials for Devices:** This part of the course focuses on the cutting-edge materials that are pivotal in overcoming the logic to memory bandwidth wall for computing applications. Participants will be exposed to a spectrum of current and emerging materials from spintronics to quantum materials, each chosen for their potential to enhance computing speed, efficiency, and data storage capabilities. Some of the topics covered include:

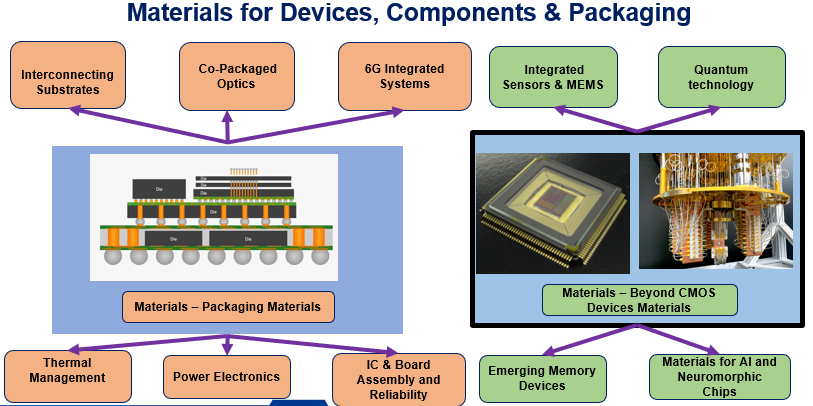
* Spintronics and ferroelectric Materials to improve memory speed and bandwidth
* Neuromorphic and Quantum Materials for future computing and AI.

**Materials for Packages:** This part of the course covers materials for package substrates, assembly of devices to package substrate, assembly of packages to the board and thermal materials.

Specific materials for substrates include metal lead frames, ceramics, glass, silicon and organic laminates. Polymer dielectrics for RDL and encapsulants and molding compounds are very commonly used. Solders constitute bulk of assembly needs at IC and board levels. In addition, heat sinks and thermal interface materials play critical roles as well.

**Materials for Components**: These are typically referred to as passive components such as capacitors, inductors and resistors. They are becoming increasingly important particularly for power management. The type of material needs are: (i) Capacitor Materials (ii) Inductor materials (iii) Resistor materials (iv) EMI shield materials

**Course for Grad Students and Industry Professionals**: This course is designed for grad-students, researchers, and professionals eager to stay at the forefront of semiconductor technology.



**Fundamentals of IC & Board Assembly and Reliability**

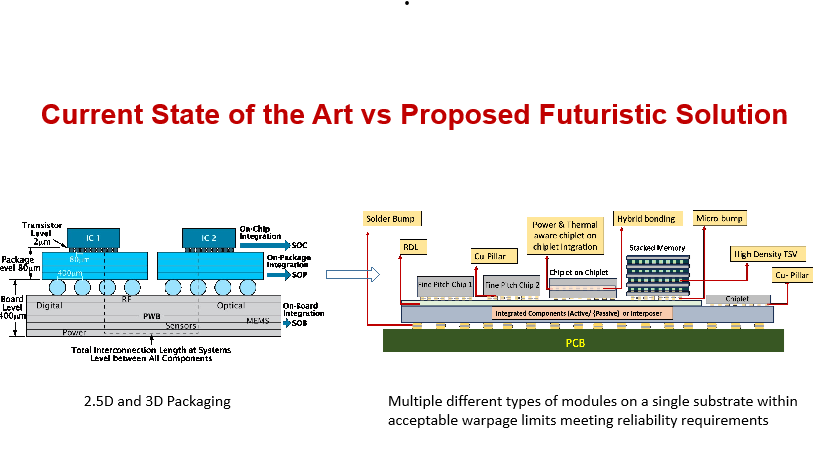
**Course Instructor:** **Prof. Nilesh Badwe, IIT Kanpur**

A person with glasses and mustache

AI-generated content may be incorrect.**Course Content:** Most people think of packaging to mean assembly of chips. Not so. What do you assemble chips to? OSAT (offshore assembly and test) companies buy wafers, dice the chips from wafers, buy substrates, assemble chips on lead-frame, organic or ceramic substrates and test electrically to make sure the chip is 100% good. The value of packaged- chip, in this process. comes from chips but the cost of assembly and test, sometimes, is as much as the chip itself. To add to that, that kind of packaging offers no increased performance, reliability or cost of the chip. So OSATs were created in lowest cost assembly countries like Malaysia, since 1980s. But all of that has changed and changing. Integrated packaging now is the highest value, more than the chip. The value now comes from integrated packaging as Moore’s law chips began to slowdown in transistor performance. So, the shift from System- On-Chip to System-on-Package has begun. Even with GPU chips that don’t have this Moore’s Law problem, the cost of multiple chips assembled on single substrate such in 2.5D architectures is cheaper than single SOCs. So, this is one paradigm shift. The 2nd paradigm shift is to do with no of I/Os required to interconnect chips with more and more transistors, currently at more than 100 Billion transistors on a single chip, requiring assembly at finer and finer I/0 pitch, currently at 9 microns, requiring non-solder-based assembly such as with Cu-Cu or hybrid bonding.

The course will cover how the assembly technology has evolved in the last 7 decades from wire bonding onto copper or Kovar lead-frames to flip chip to micro-bmp to thermocompression bonding-- all using solders to solderless direct copper to copper or hybrid bonding enabling sub-10 m pitch. However, hybrid invented by Ziptronics more than 25 years ago was developed for assembly to silicon substrates. But glass substrates pioneered by Georgia Tech team are going into manufacturing to replace silicon in future. The course will also highlight the progress in the board- level assembly with a case study on low temperature solders with a primary focus on improved reliability through material design. The course will also cover basics of reliability including accelerated tests such as thermal cycle/shock, mechanical shock, and electromigration.

**Course for Grad Students and Industry Professionals:** This course is designed for both undergraduate and graduate students as well as working professionals. The course will introduce participants to the fundamentals of IC & board assembly and reliability.

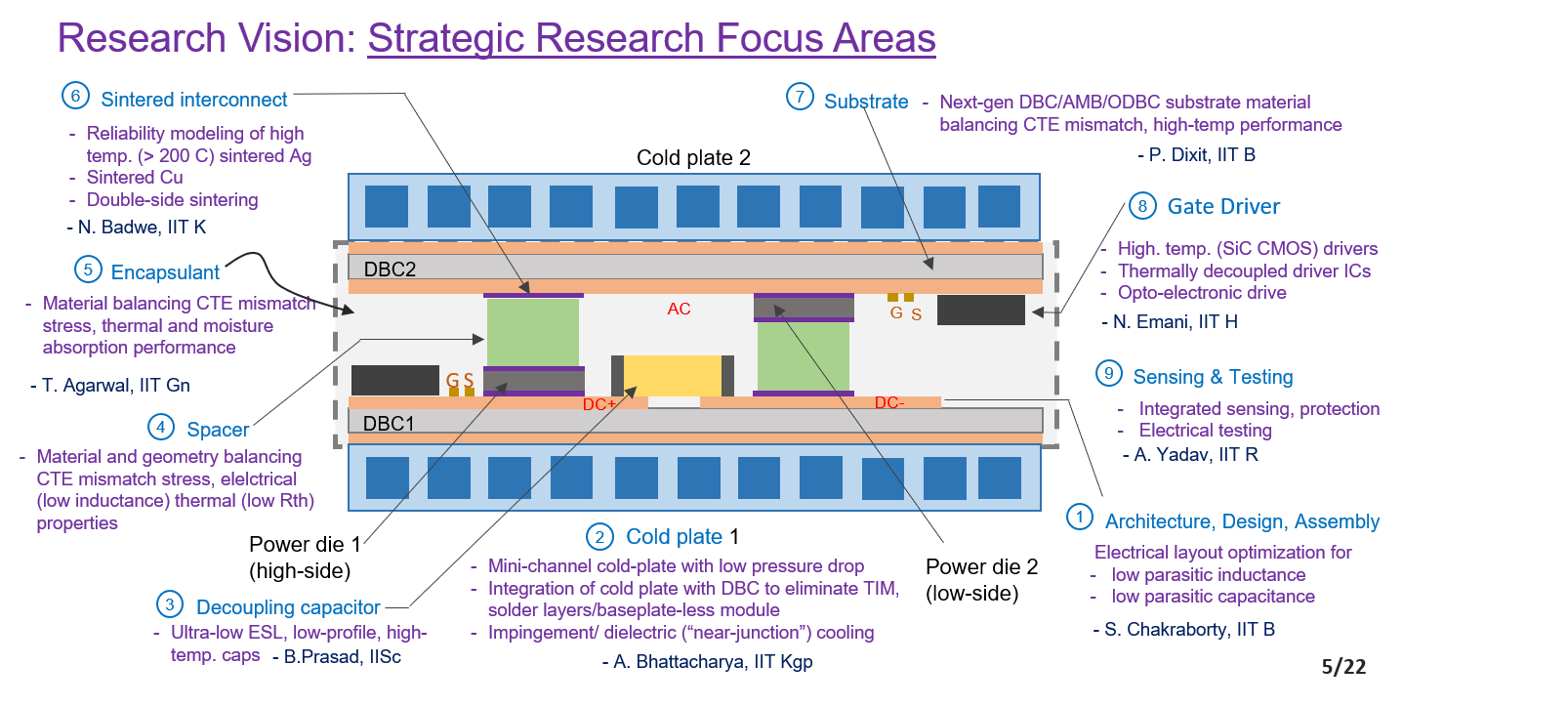


**Fundamentals of Power Electronics Packaging**

**Course Instructor: Prof. Shiladri Chakraborty, IIT Bombay**

**Course Content:** Improvements in the electrical switching performance, losses, and thermal management of power semiconductor devices are key enabling pathways to meet the ever-increasing demands of improved power-density in power electronic converters, such as EV traction inverters. With recent innovations in power semiconductor device technology, particularly wide-bandgap (WBG) compound semiconductor devices, the role of device and systems packaging has become increasingly more vital to fully leverage the benefits of such devices.

This tutorial will cover the fundamentals of legacy power electronics packages and review recent developments in WBG power device packaging. The session will start with a description of the basic architectures and functioning of conventional power electronics modules and explain why WBG devices cannot be used as drop-in replacements in conventional Si-device packages. State-of-the art packaging approaches from academic literature and industry products enabling enhanced electrical performance of WBG devices will be reviewed, along with strategies for improvements in thermal management and reliability. System-level trade-offs across the different domains will also be emphasized, highlighting the need for multi-physics, multi-objective design optimization automation. Finally, future trends in different constituent technology areas will be discussed.

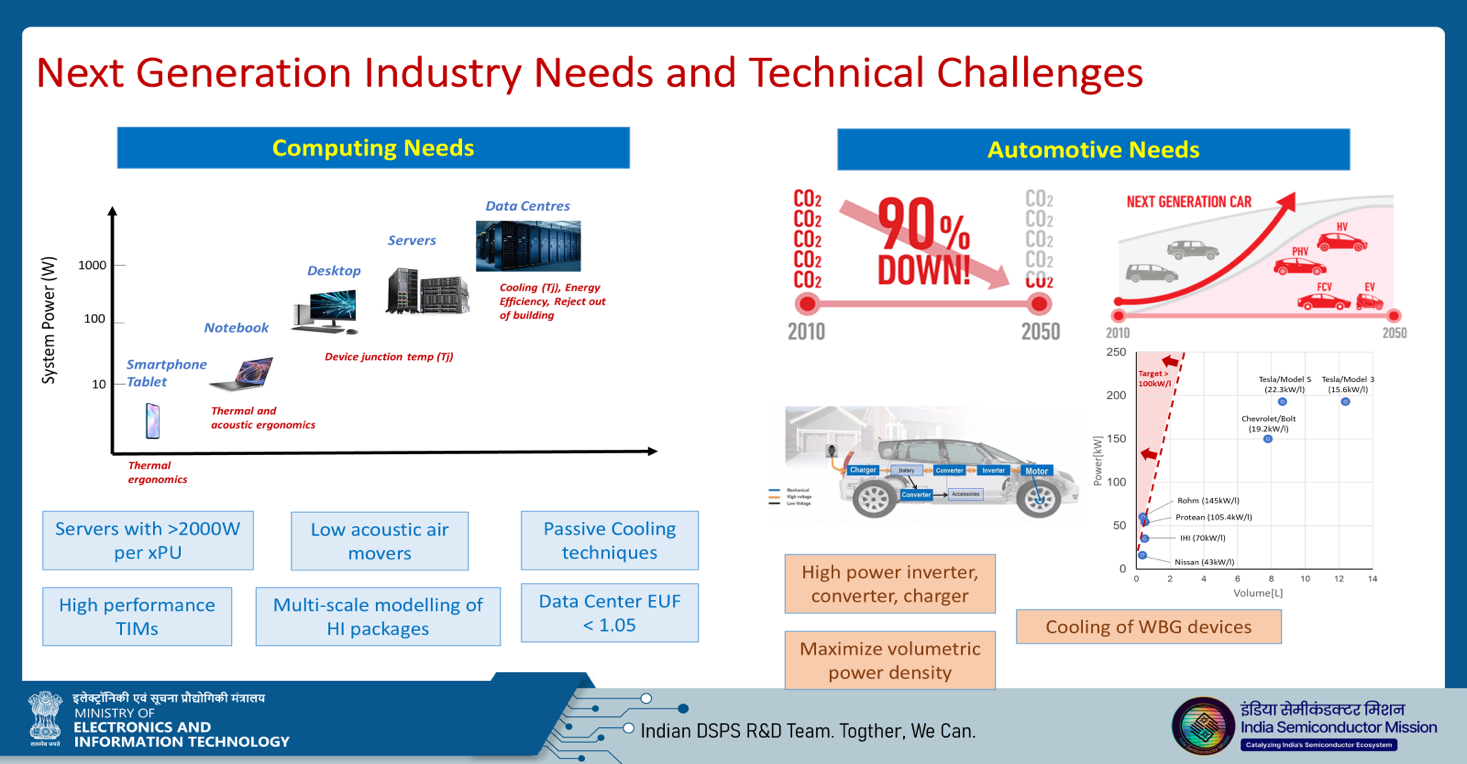
**Course for Grad Students and Industry Professionals:** The course is designed to benefit beginners in power electronics systems packaging, offering insights into essential foundational concepts, as well as advanced engineers seeking to stay informed about the latest developments in the field.

**Fundamentals of Thermal Management**

**Course Instructor: Prof. Anandaroop Bhattacharya, IIT Kharagpur**

**** **Course Content**: The large-scale integration of more and more transistors within a chip, on one hand, and integration of more and more chips on individual packages such as in 2.5D,3D and emerging chiplet architectures, on the other hand, coupled with continuous push for increased electrical performance, continues to result in steep increase in heat dissipation rates across many applications. This, in turn has called for continuous innovation and development of novel thermal technologies across all product segments from smartphones to data centres in the computing world, and from LED lights to high performance power modules for electric cars in the automotive world.

This short course is designed to provide an overview of the thermal challenges faced by the semiconductor industry, and some of the fundamental cooling technologies developed to address these challenges. The course also covers some recent advances in this domain. The course will begin with the fundamental modes of heat transfer, followed by the basic terminologies and definitions that are used in thermal design and cooling solutions. We will then move to the fundamental cooling solutions viz. finned heat sinks, heat pipes, liquid pumped loop and refrigeration systems, with a specific case study on the design of a parallel plate finned- heat sinks coupled with a fan. The course will finally end with some recent advances in both the computing and automotive sectors as well as some specific next gen research challenges.

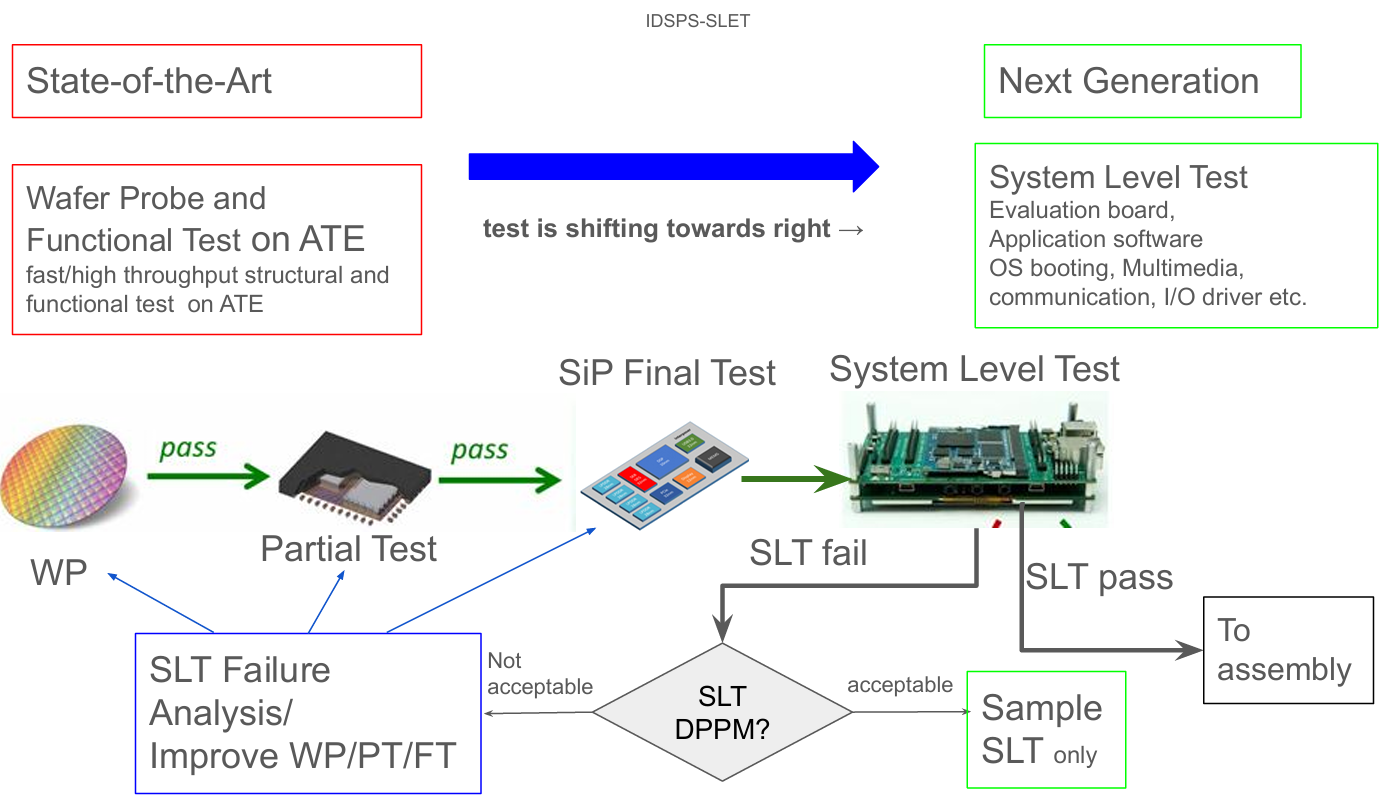
**Course for Grad Students and Industry Professionals**: This course is designed for graduate students, researchers, and professionals eager to stay at the forefront of semiconductor and packaging technologies. By the end of this course, participants will have a good understanding of the metrics for a good thermal design, thermal challenges across the computing and automotive electronic sectors, both at device and system levels, the technologies that are currently used and the design philosophy behind them.

**Fundamentals of System Level Electrical Test**

**Course Instructor: Prof. Jaynarayan T Tudu, IIT Tirupati**

**Course Content**: The progress in device, packaging, systems technologies has become so complex and is beginning to pose newer challenges as their integration takes hold. The traditional structural or functional test alone is not sufficient to test the defects in such technologies. The defects that escape either the structural or functional tests have been observed to appear at the system level as error or failure. Therefore, the modern complex systems have to be tested at the system level in addition to the traditional tests at each level. Further the changes in integrated packaging technologies are bringing newer challenges in 2.5D/3D SiP tests. Newer standard IEEE P3405 is in progress to deal with the upgraded boundary scan architectures for chiplet-based packaging. The critical application’s need for zero defects and DPPM problem are being addressed in a newer way as a known good chiplet (KGC).

The syllabus for this course will cover the test technology, as it has evolved over time. It consists of design for testability, ATPG algorithms, and ATE test methodology. The various fault models will be discussed covering the recent challenges in open and short defects and the cell aware test. ATPG algorithms and application of machine learning algorithms in tests will also be discussed. The scan-based architecture will be reviewed in light of modern chiplet- based design and AI accelerator. The research challenges in reducing the test cost, data volume, test time and power consumption will be discussed.

**Course for Grad Students and Industry Professionals**: This course is designed for students, researchers, and professionals eager to stay at the forefront of integrated semiconductor test technology. By the end of this course, the graduate students will have a research problem in hand to solve. The industry professionals will get the updated- knowledge on the recent technological advances in system level tests along a vision for the future of test technology.